High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics

Doug Barlage, Reza Arghavani, Gilbert Dewey, Mark Doczy, Brian Doyle, Jack Kavalieros, Anand Murthy, Brian Roberds, Pat Stokley and Robert Chau

Components Research

Logic Technology Development

Intel Corporation

Outline

- Motivation
- Measurement Challenges
- Fabrication
- Device Results
- Testing Methodology
- Dielectric Constant Test Results
- High Frequency Benchmark
- Conclusions

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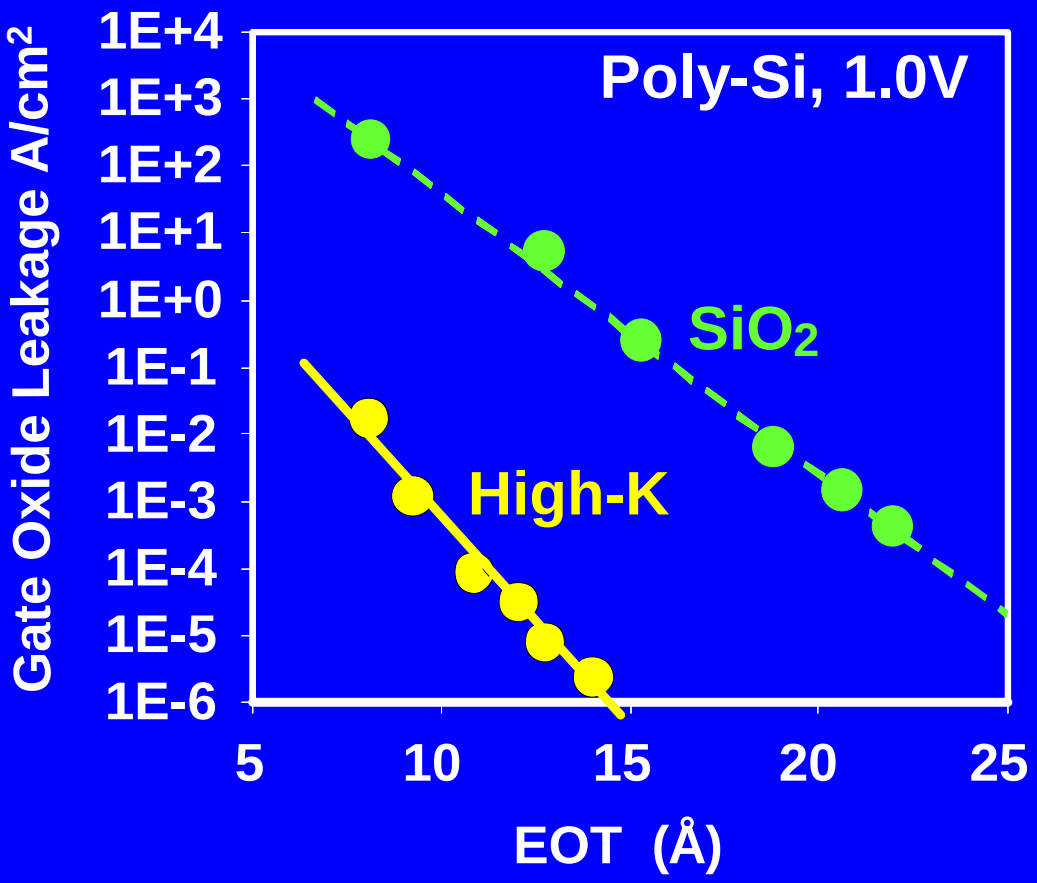
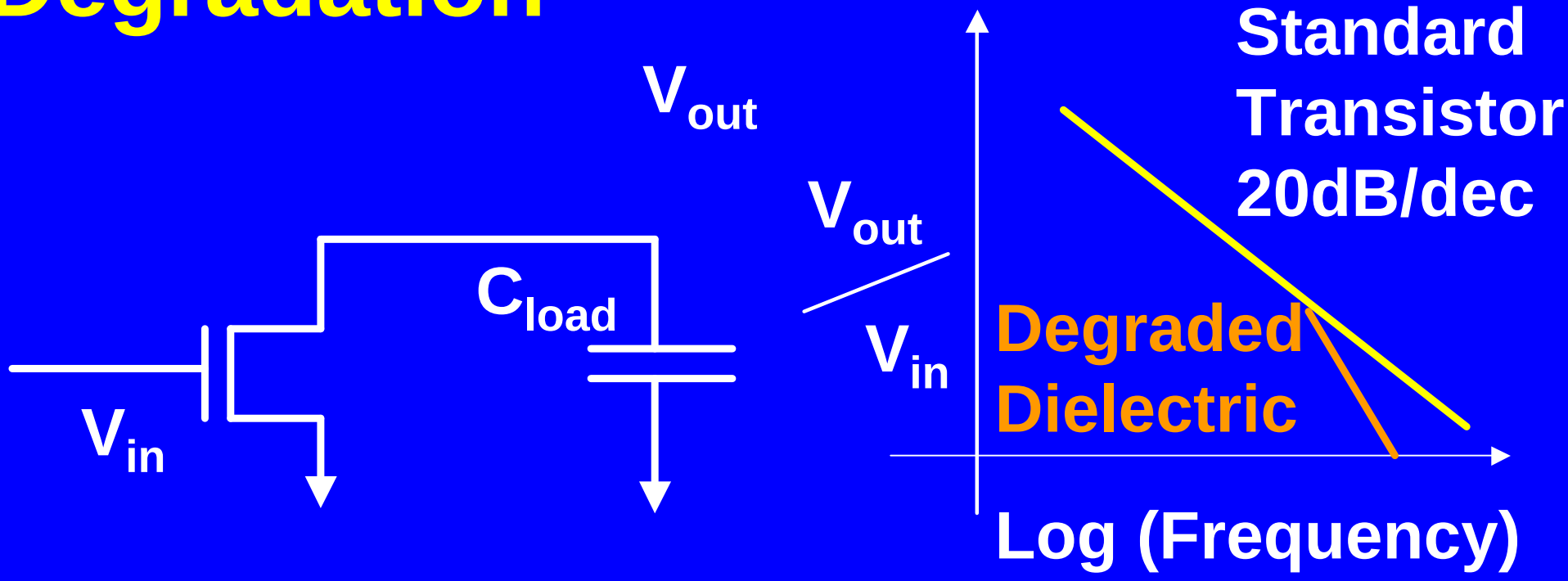
Motivation – Aggressive Scaling



- **Future generations of microprocessors will require high-K gate dielectric**

Motivation – Transistor Degradation



- The ability to drive a load at high speed will be lost if the dielectric constant degrades as a function of frequency

Motivation

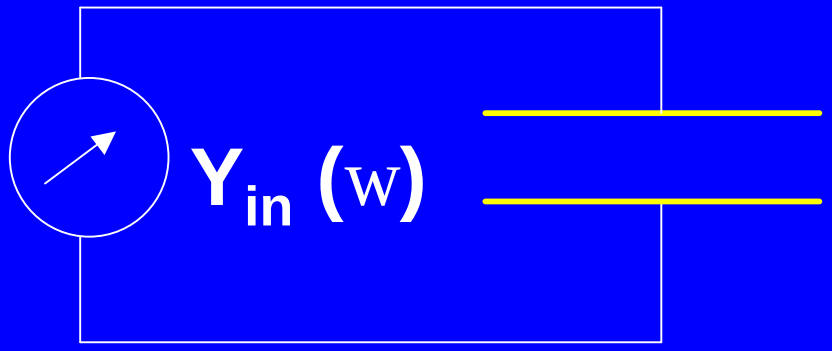
- Some “Super high-K” (K > 100) materials are known to have poor dielectric constant frequency $\varepsilon(f)$ response[1]

- Do gate dielectric (3.9 < K < 30) materials such as HfO_2, ZrO_2 and SiO_2 exhibit poor dielectric response?

[1] McNeal, M.P., IEEE ISAF 1996, pp. 18-21 Aug. 1996.

Measurement Challenges – Ideal Capacitor

$$Y = \frac{A}{t} \bullet (2pf \cdot e(f)) \bullet (\tan(\partial) + j)$$



Thin film capacitor

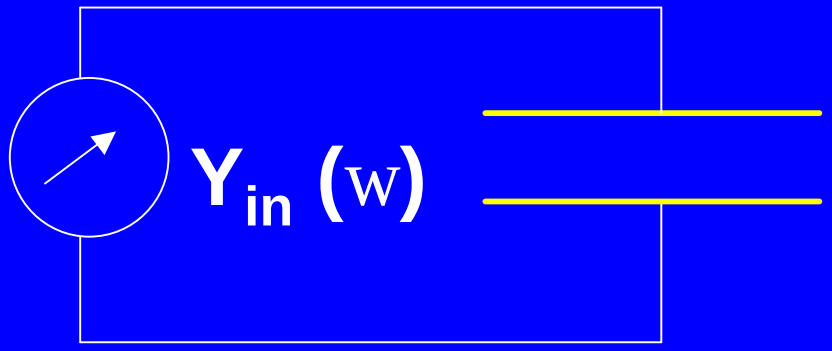
$$e(f) = \frac{\mathrm{Im}(Y(f))}{A/t \bullet 2pf} = \frac{C_{meas}}{A/t}$$

$$\tan(\partial) = \frac{2pfe'' + s + \frac{\partial J_{ox}}{\partial V} \bullet t}{2pfe(f)}$$

- **Admittance measurement of pure capacitor can be evaluated at high frequency**
- **e(f) can be determined from the measured capacitance**
- **Thin film challenges**

Measurement Challenges – e(f) calculation

$$Y = \frac{A}{t} \bullet (2pf \cdot e(f)) \bullet (\tan(\partial) + j)$$



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- Admittance measurement of pure capacitor can be evaluated at high frequency
- e(f) can be determined from the measured capacitance
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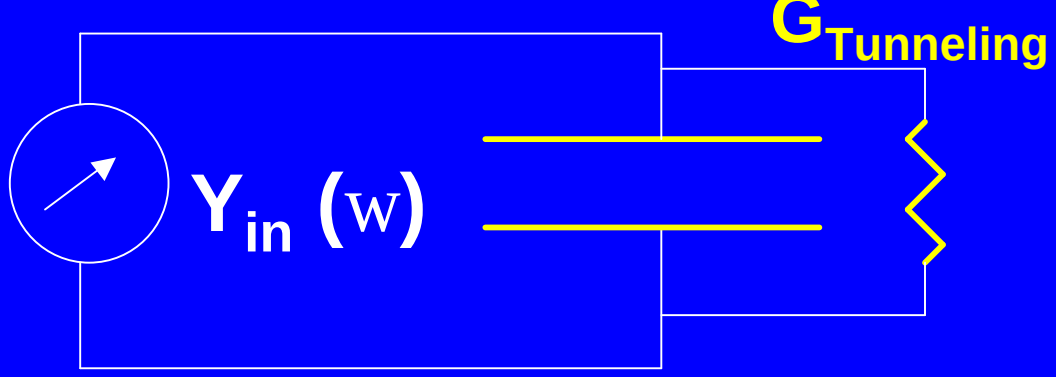
Measurement Challenges – Tunneling Leakage

$$Y = \frac{A}{t} \bullet (2pf \cdot e(f)) \bullet (\tan(\partial) + j)$$



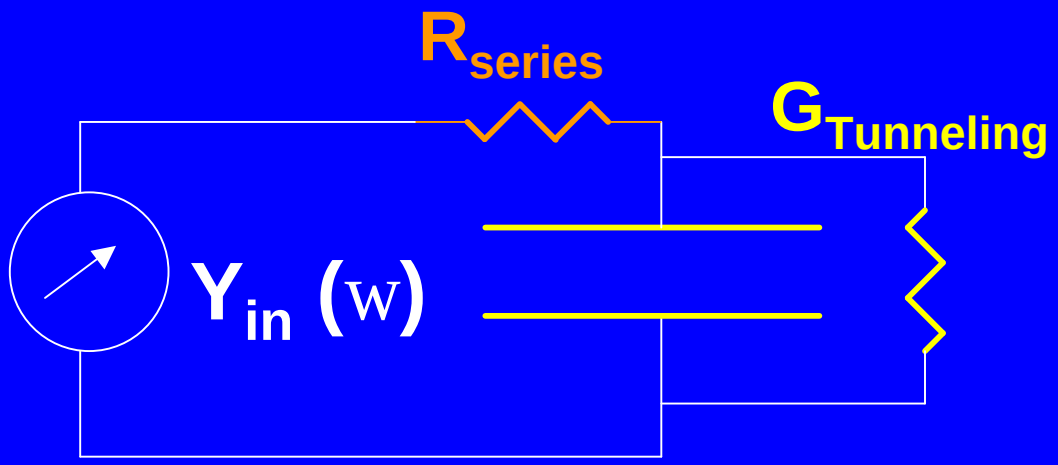
$$e(f) = \frac{\mathrm{Im}(Y(f))}{A/t \bullet 2pf} = \frac{C_{meas}}{A/t}$$

$$\tan(\partial) = \frac{2pfe'' + s + \frac{\partial J_{ox}}{\partial V} \bullet t}{2pfe(f)}$$

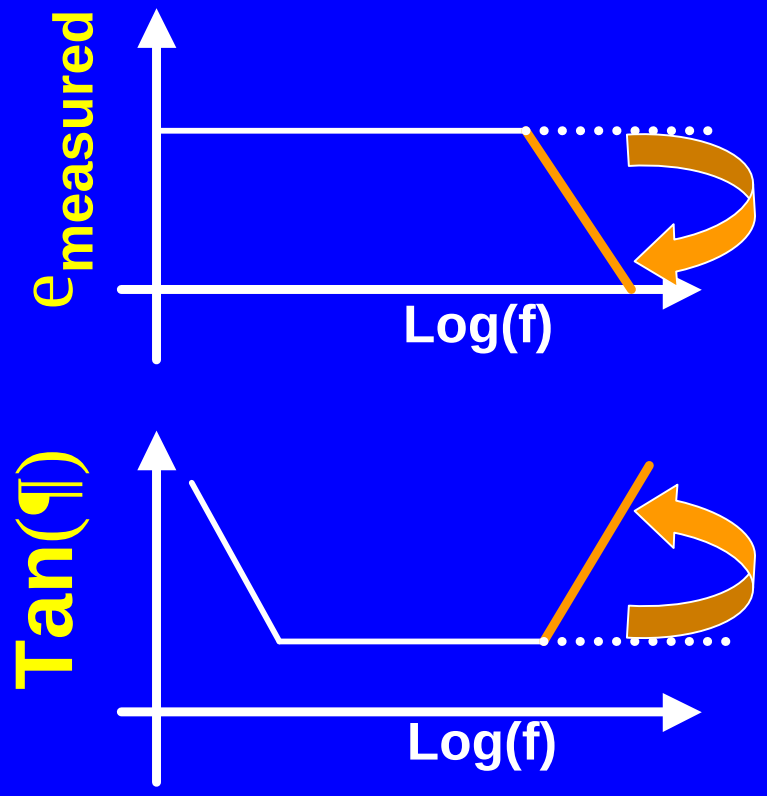
Thin film capacitor With Leakage

- Admittance measurement of pure capacitor can be evaluated at high frequency
- e(f) can be determined from the measured capacitance
- Thin film challenges – Tunneling leakage

Measurement Challenges -- Non-Ideal Capacitor



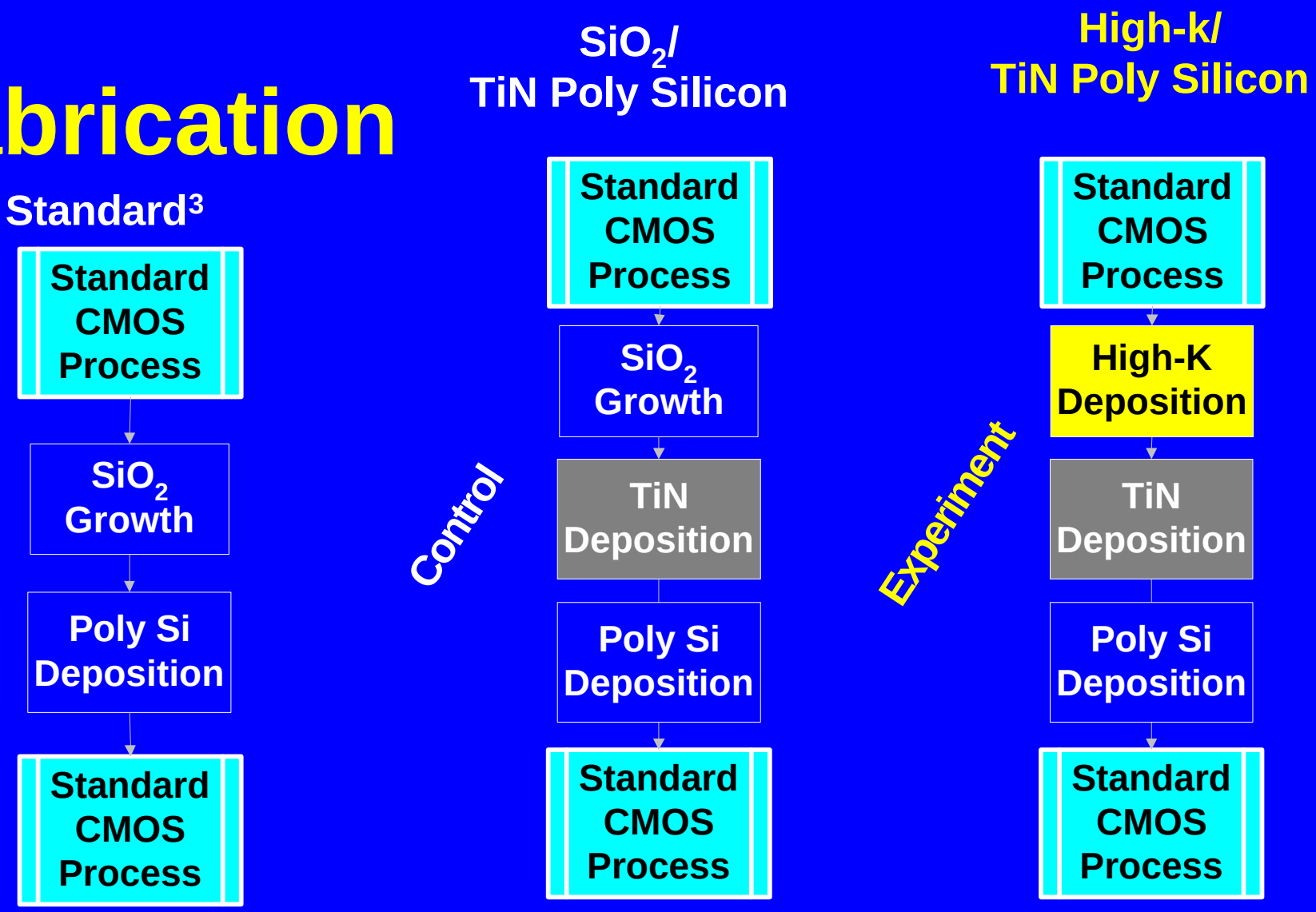
Perfect e thin film capacitor



- Thin film challenges
  - Series resistance convolutes measurement at high frequency[2]
  - This work introduces a methodology to circumvent this problem by minimizing all external resistance

[2] D. W. Barlage et. al., Electron Dev. Lett, pp. 454-456. Sep. 2000

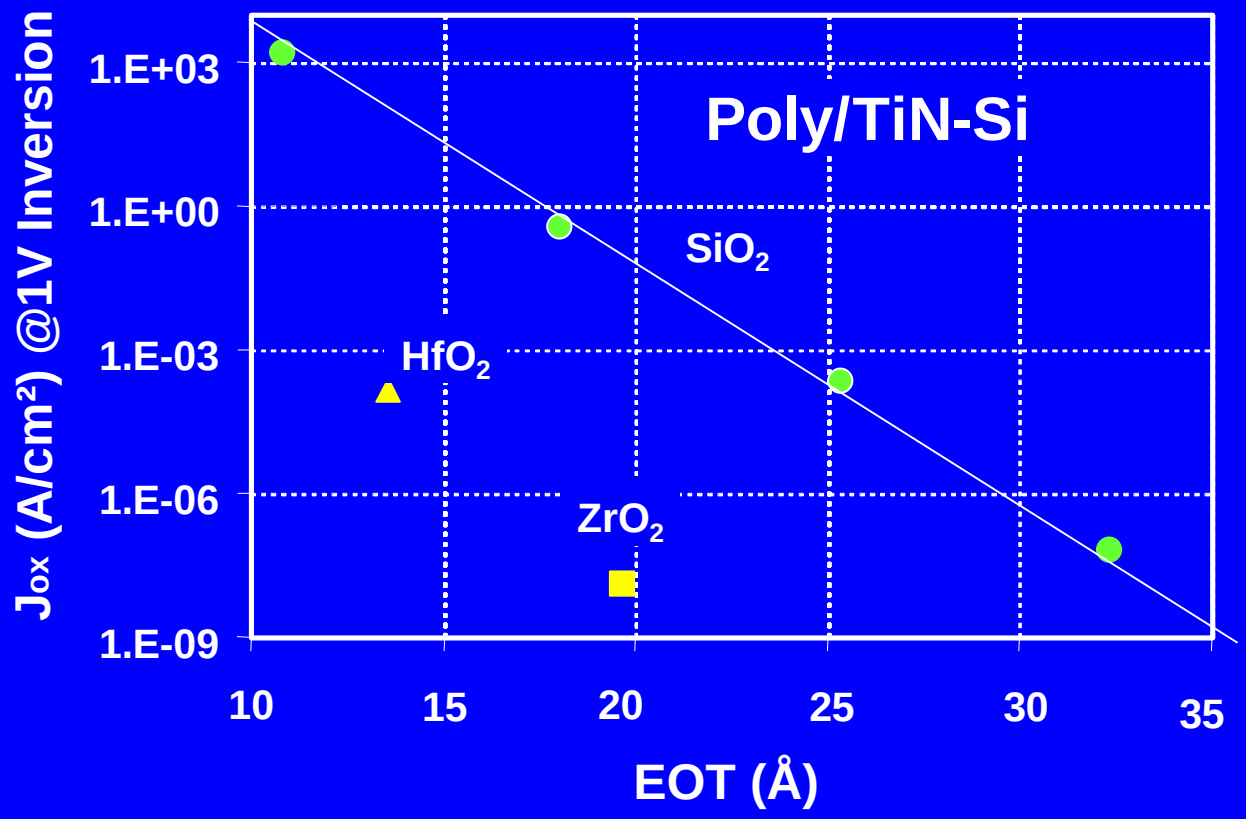
Fabrication



- **Standard process flow[3] except for gate stack**

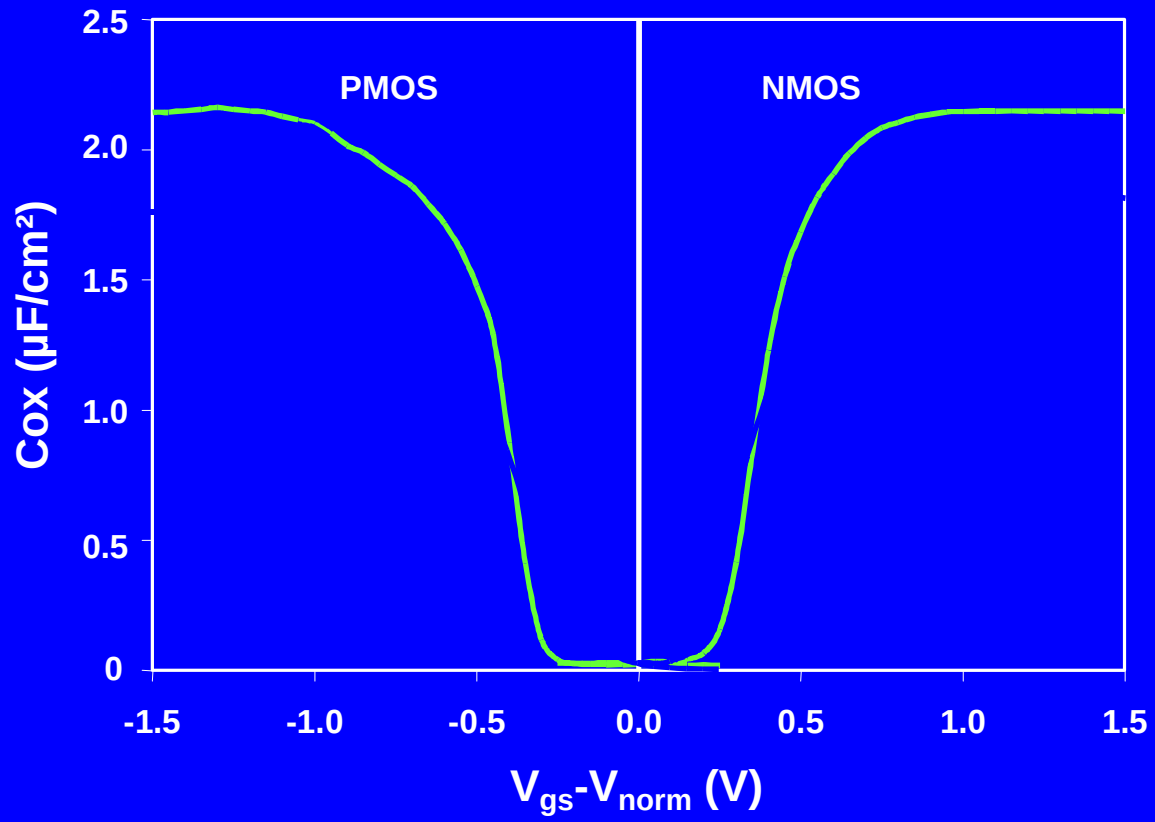
[3]S. Tyagi et. al., 2000 IEDM, pp 567-570, Dec. 2000.

Device Results - Gate Leakage



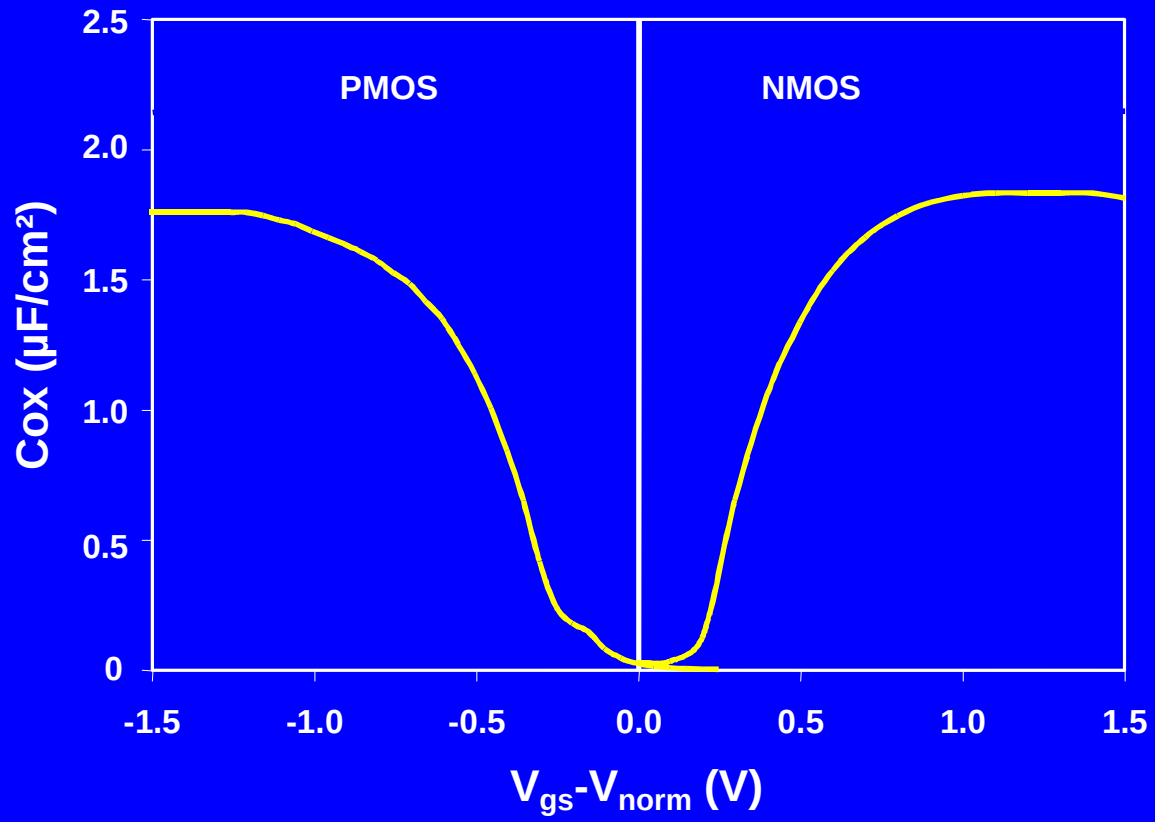
- **Samples in this study indicate high-K has over 5 orders of magnitude leakage reduction over SiO_2**

Device Results – SiO_2 Gate C-V



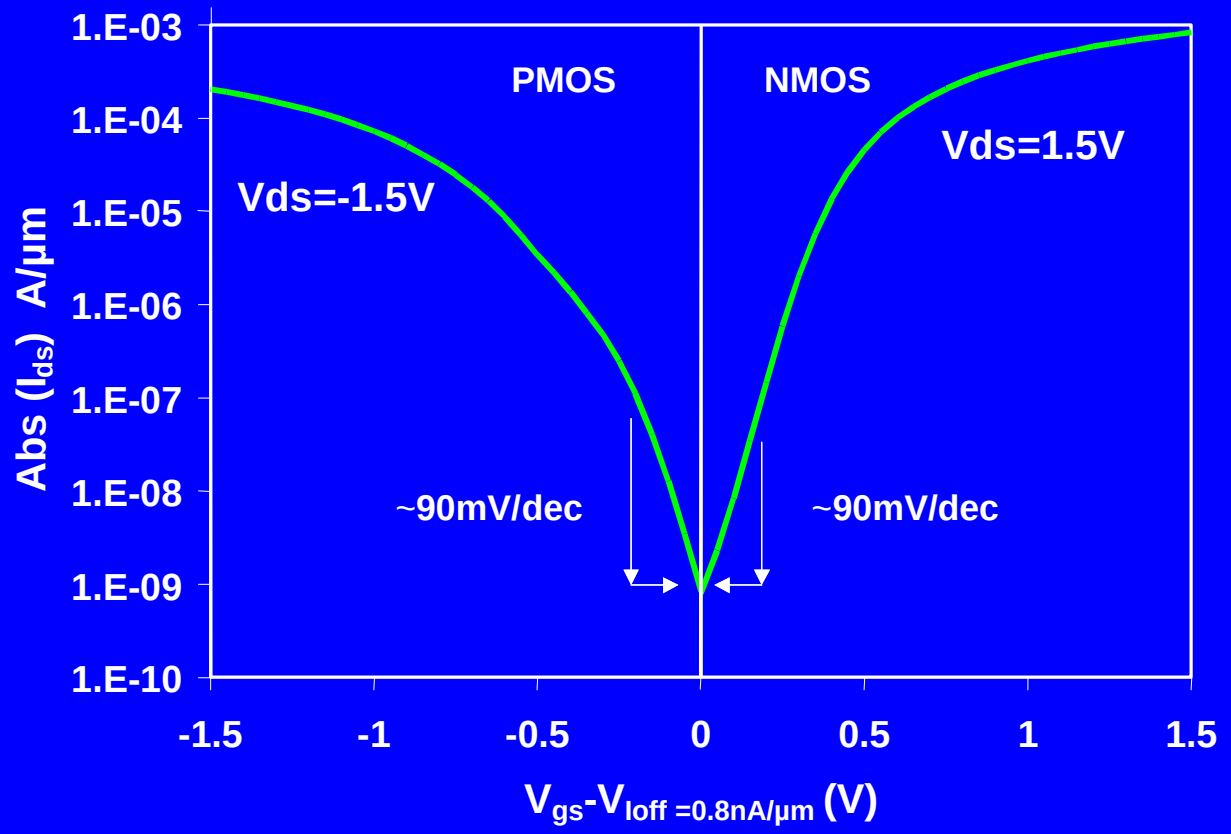
- Inversion C-V curve of both PMOS and NMOS shows healthy results for the SiO_2
- C_{ox} maximum is greater than 2.2µF/cm^2 for NMOS and PMOS

Device Results – high-K Gate C-V



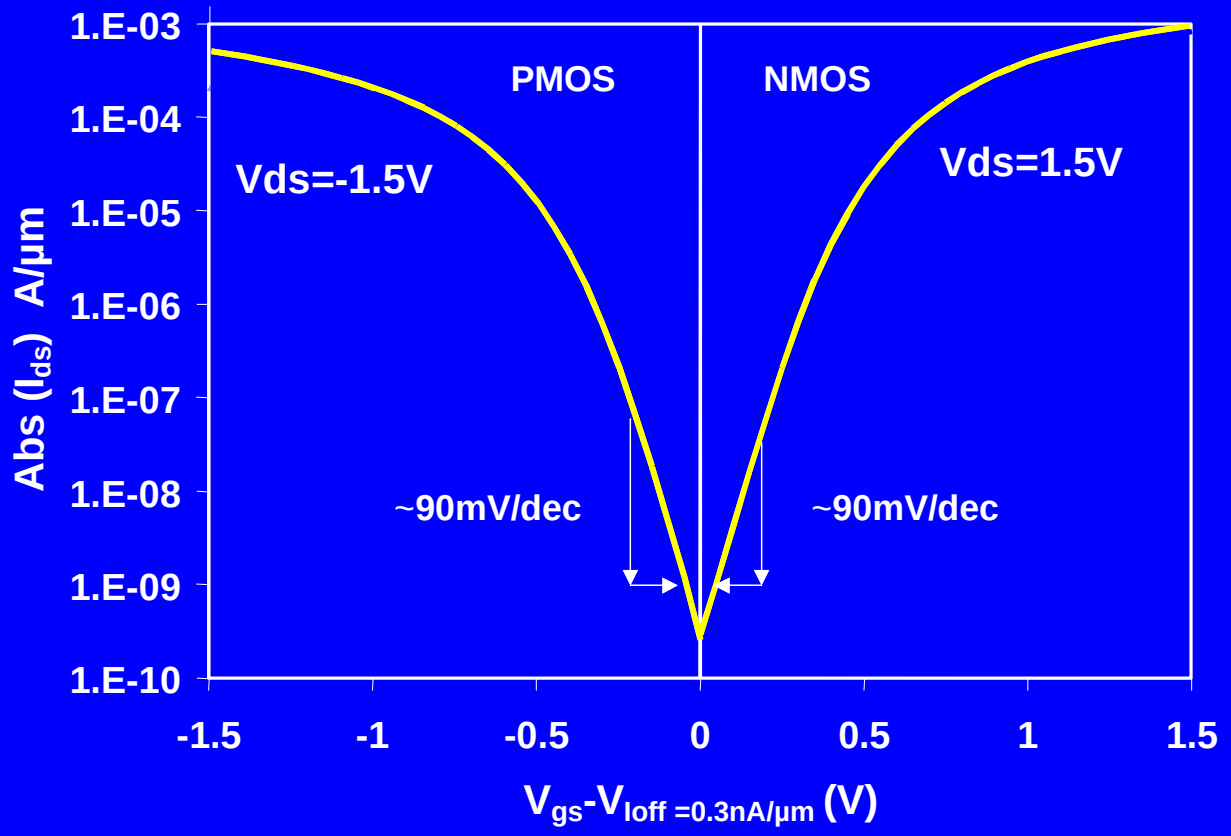
- Inversion C-V curve of both PMOS and NMOS shows healthy results for the high-K
- C_{ox} maximum is greater than 1.7µF/cm² for NMOS and PMOS.

Device Results – SiO_2 I_{ds}-V_{gs}



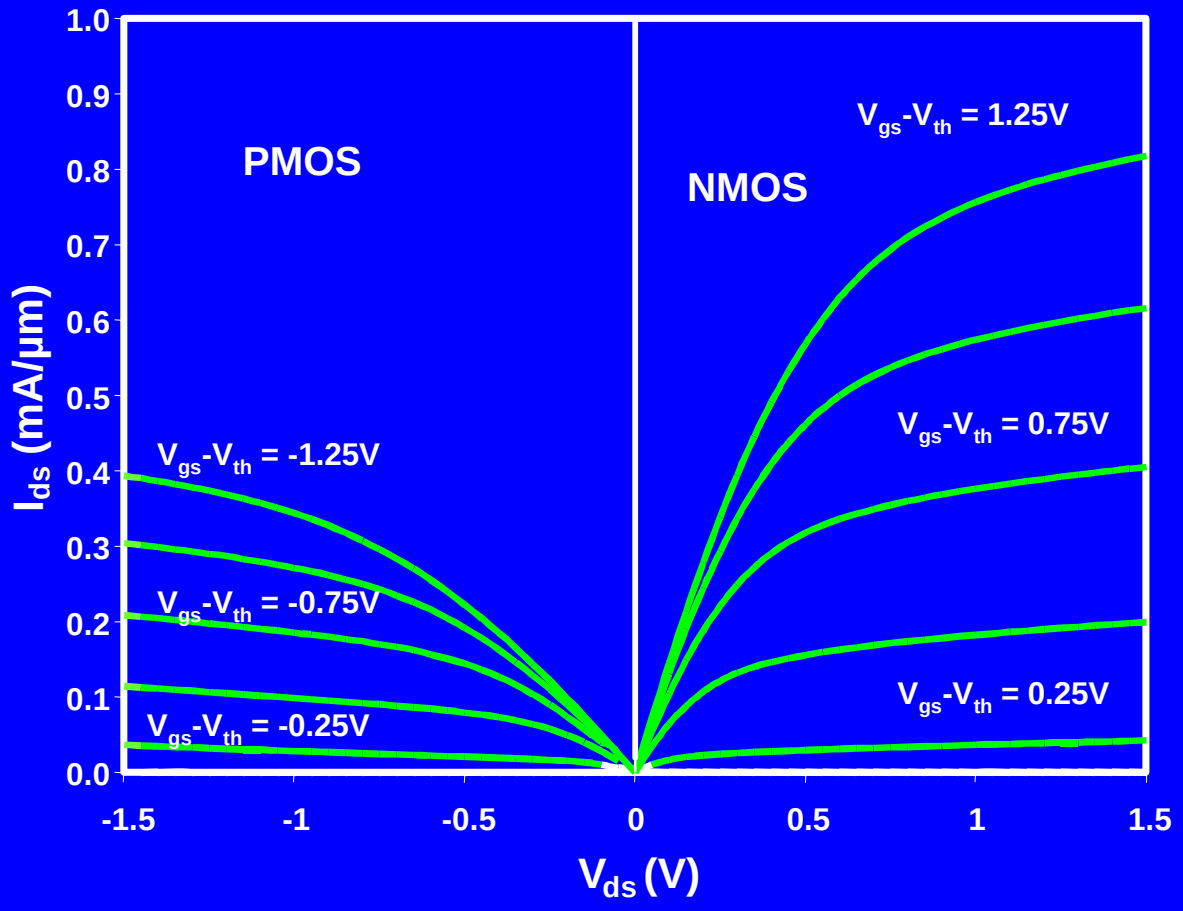
- SiO_2 TiN/Poly sample exhibits good sub-threshold slope and drive current

Device Results – high-K I_{ds}-V_{gs}



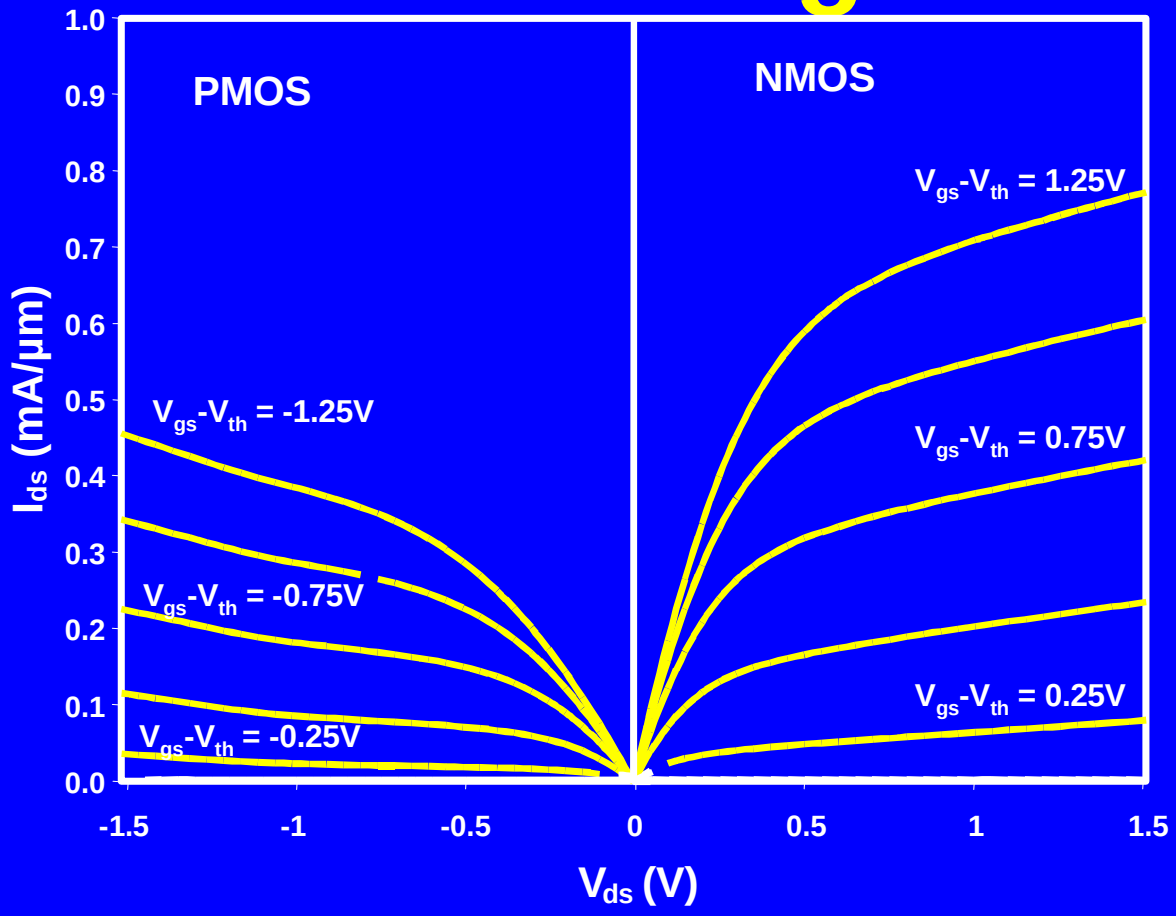
- High-k TiN/Poly sample exhibits good sub-threshold slope and drive current
- Similar characteristics to the SiO_2 with TiN case

Device Results – SiO_2 Family



- The SiO_2 family of curves shows good drive current for 100nm Gate length

Device Results – high-K Family

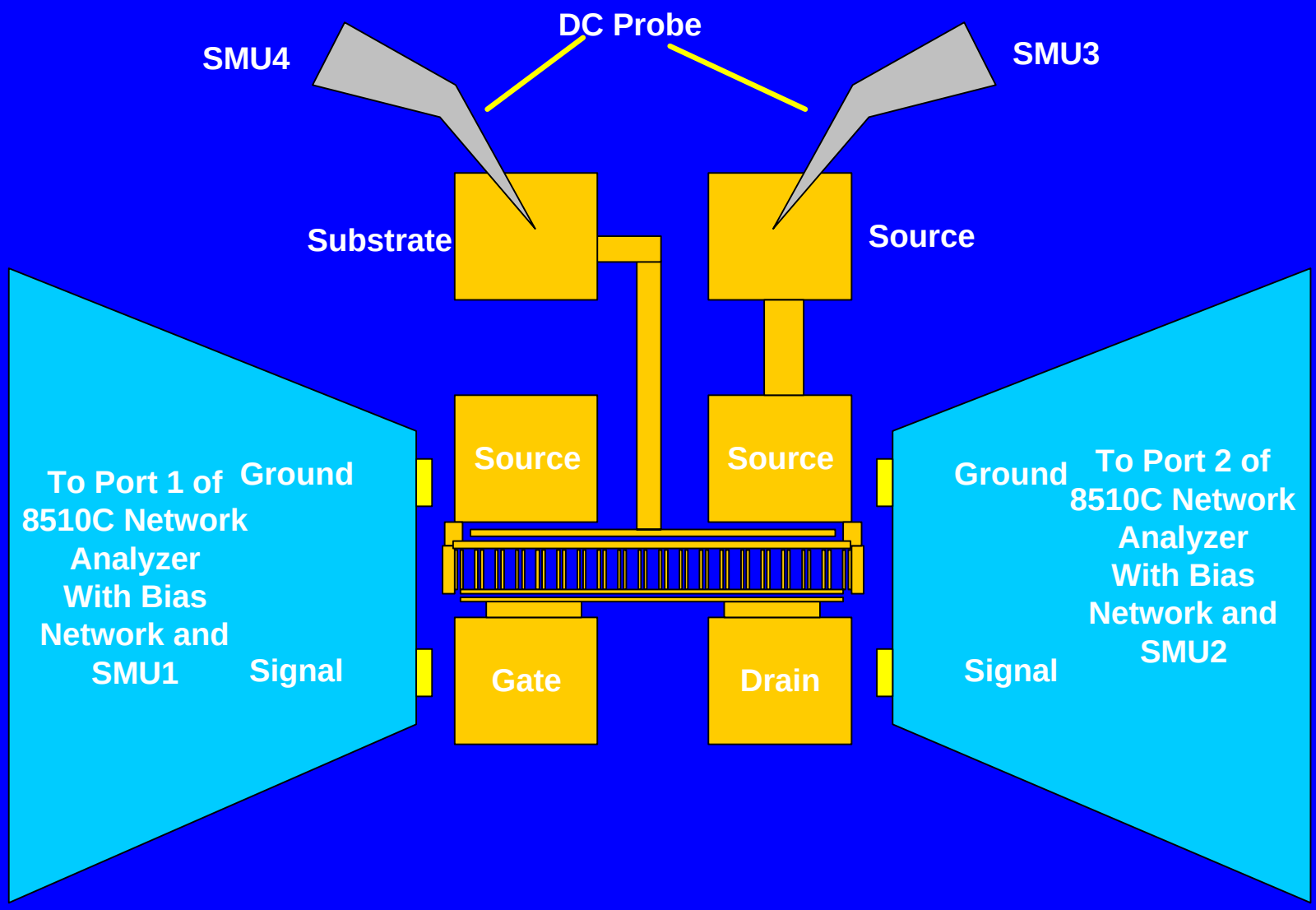


- The high-K family of curves shows good drive current for 100nm Gate length

DC Results -- Summary

- High quality film is achieved
- Similar results for high-K and SiO_2 devices

High Frequency Measurement



Testing Methodology – Minimizing the RC time Delay

$$\text{Maximum Measurement Frequency} \sim \frac{1}{2\pi \bullet \tau_{RC}}$$

$$\tau_{RC} = \tau_{RCB} + \tau_{RCW} + \tau_{RCL}$$

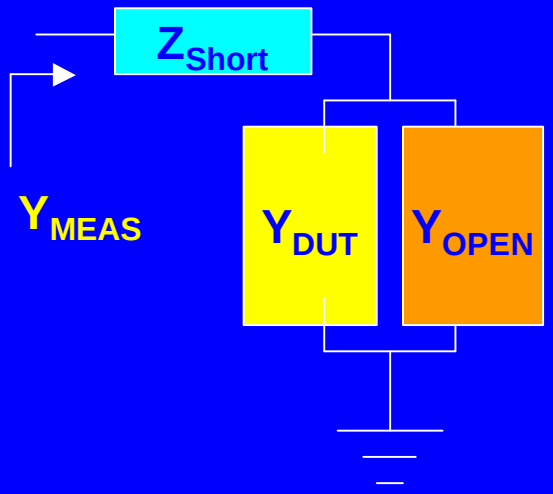
Bussing

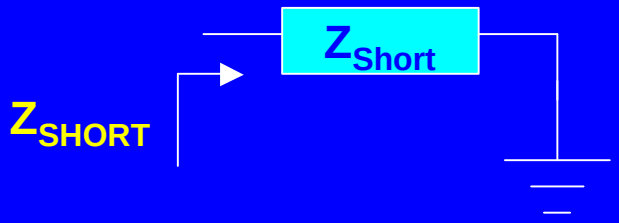
Gate Width

Gate Length

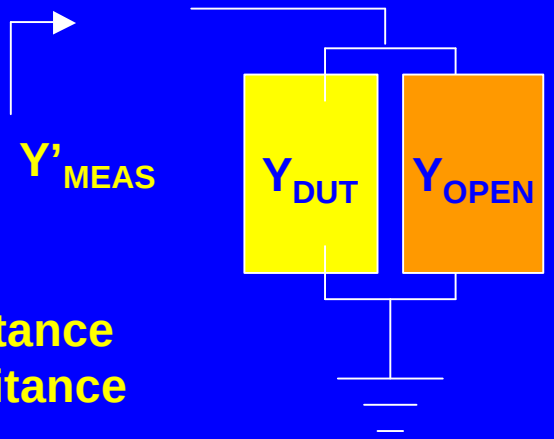
- **Minimize the total RC constant to maximize meaningful measurement Frequency**
  - **RC from Bussing**
  - **RC from Gate Width**
  - **RC from Gate Length**

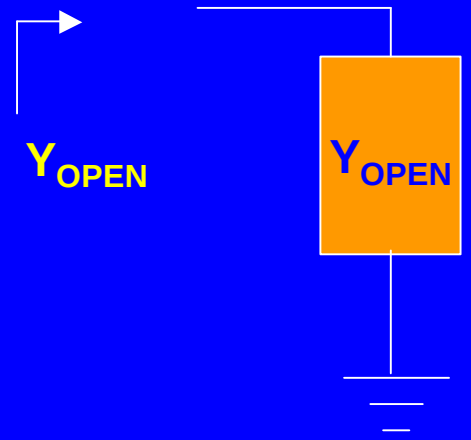
Testing Methodology – on wafer Open Short Cal



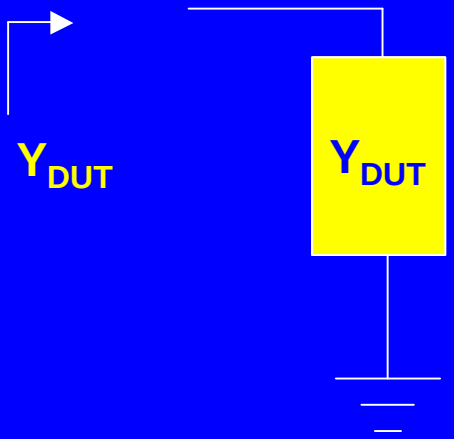


$$Y'_{MEAS} = [1/Y_{MEAS} - Z_{SHORT}]^{-1}$$





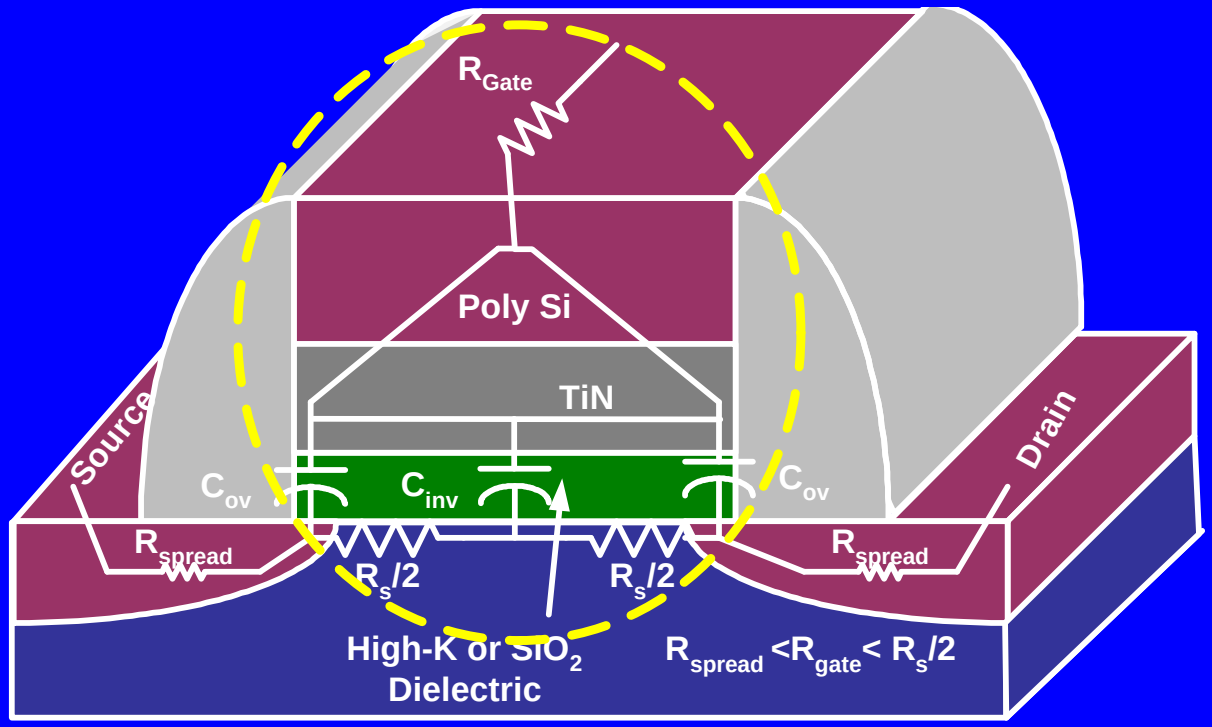
$$Y_{DUT} = Y'_{MEAS} - Y_{OPEN}$$



Z_{SHORT} comes from pad/bus resistance
Y_{OPEN} comes from pad/bus capacitance

- **Minimize the total RC constant to maximize meaningful measurement Frequency**
  - **RC from Bussing – On wafer open-short calibration**
  - **RC from Gate Width**
  - **RC from Gate Length**

Testing Methodology

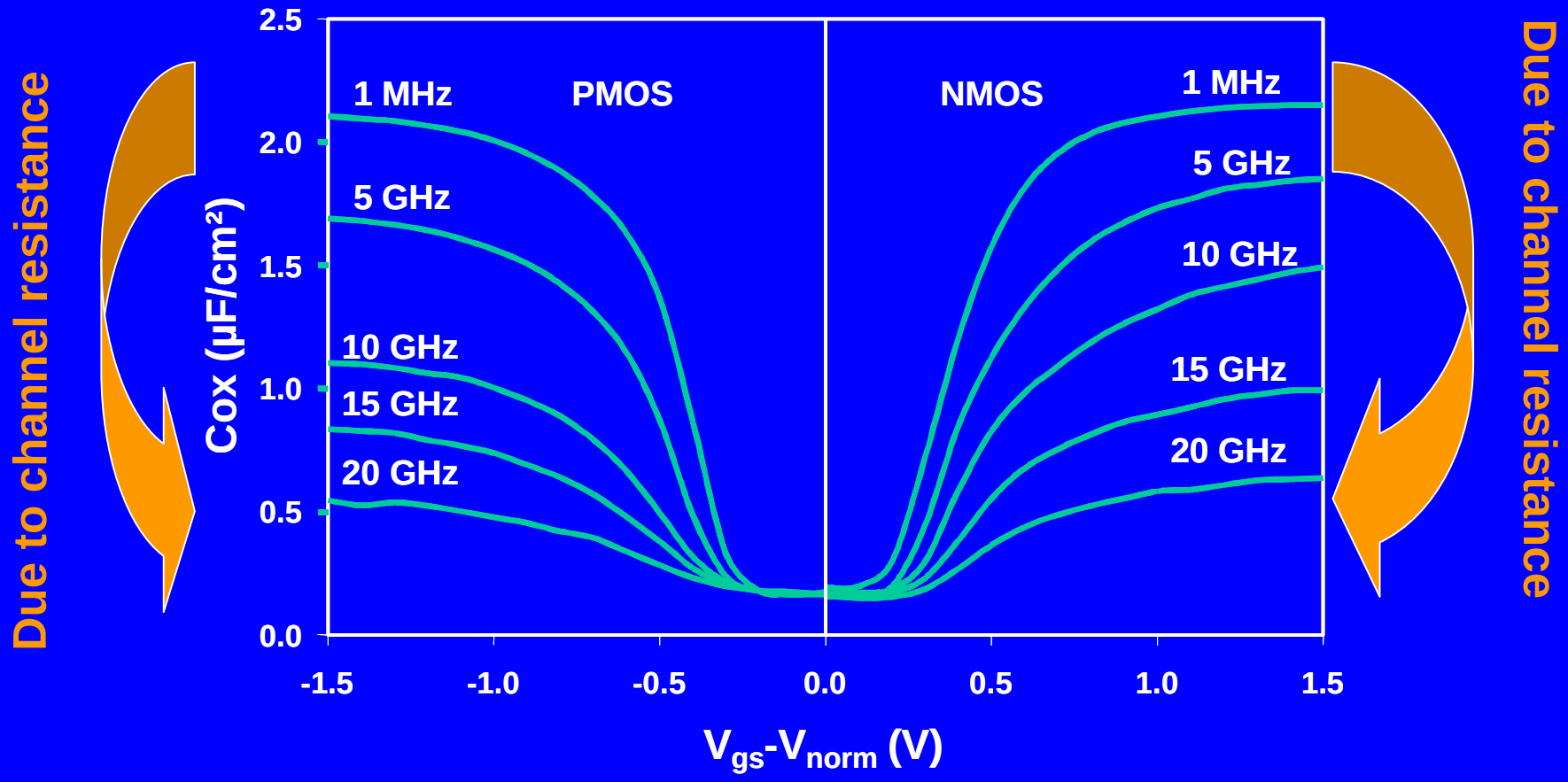


Minimize R_g
L_g ~ 1 µm
W_g < 10 µm

Minimize R_g
L_g ~ 1 µm
W_g < 10 µm

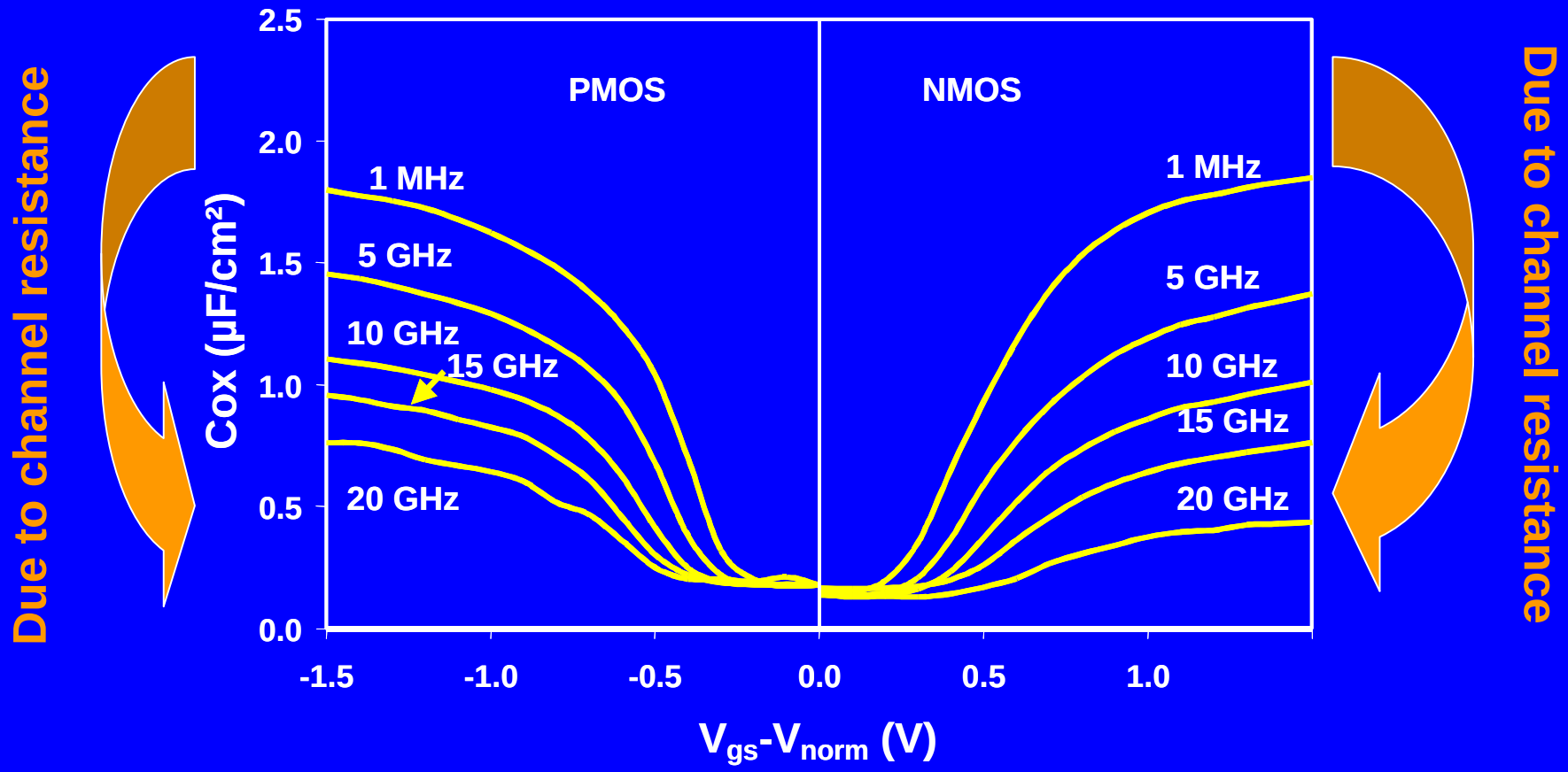
- Minimize the total RC constant to maximize meaningful measurement Frequency
  - RC from Bussing – On wafer open short calibration
  - RC from Gate Width – Use small gate width and larger gate length
  - RC from Gate Length

High Frequency CV Curve – SiO_2



- Typical inversion CV curve of 1μm gate length with SiO_2 gate stack structure taken at high frequencies shows degradation at high frequency

High Frequency CV Curve – High K



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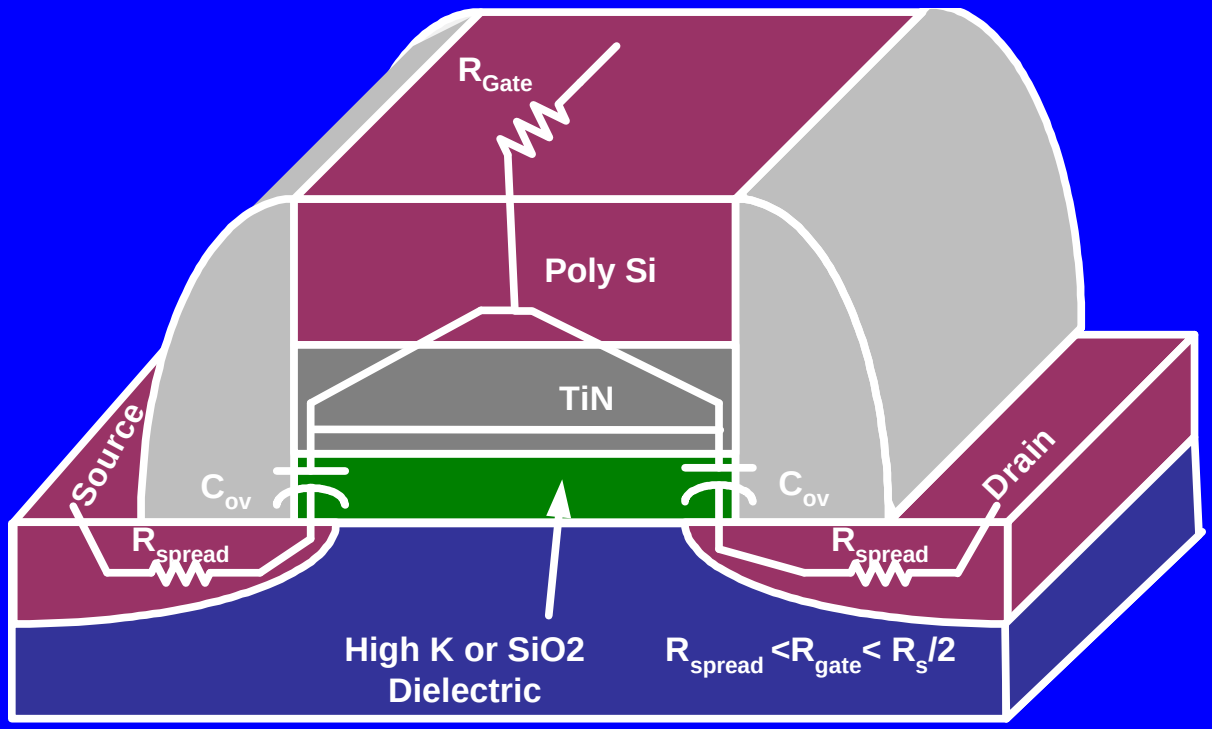
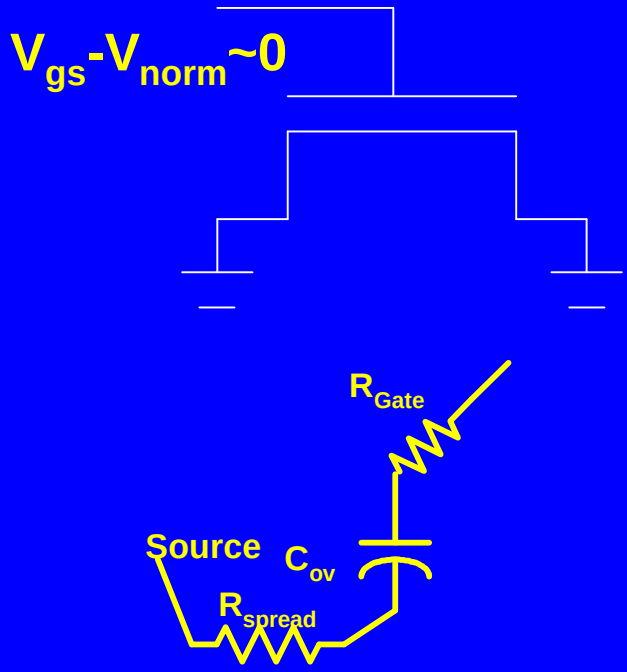


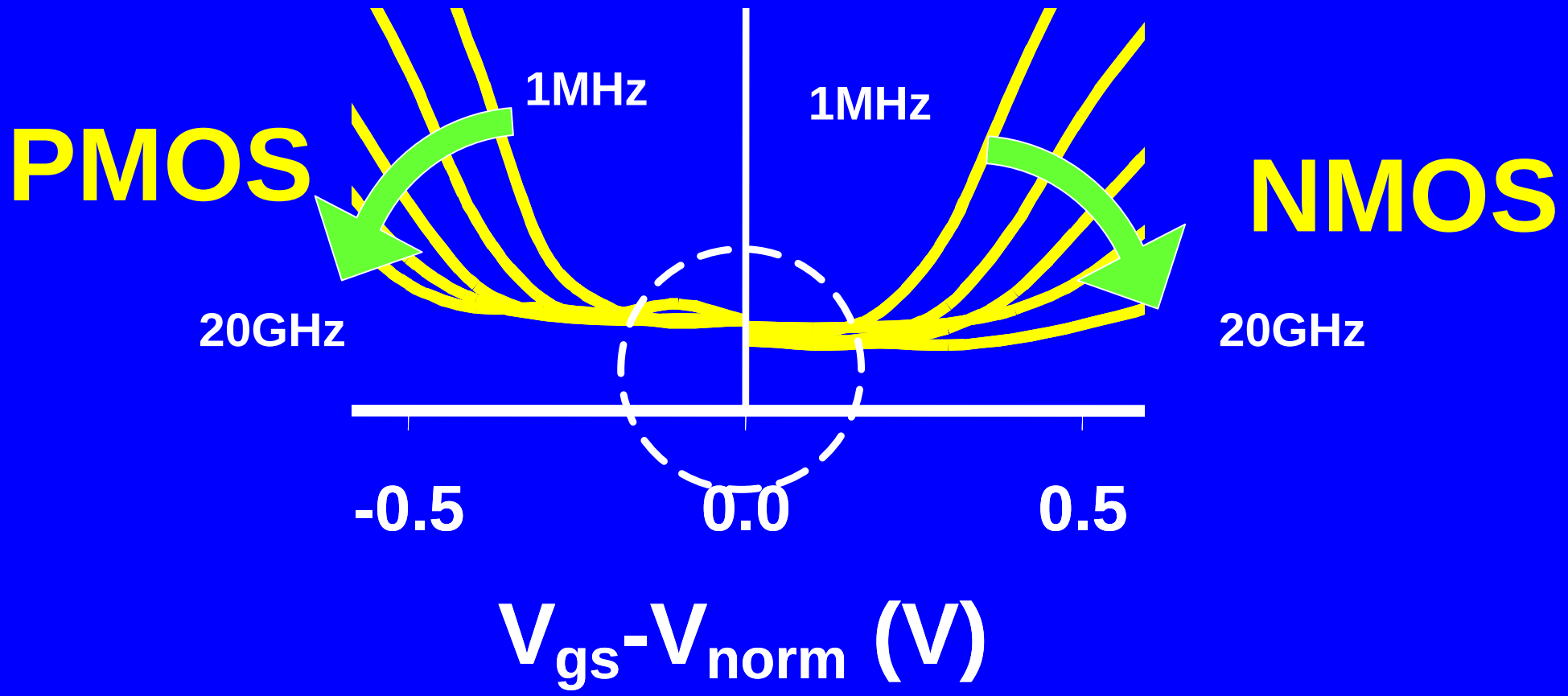


Eliminate gate length resistance by measuring only overlap capacitance

-

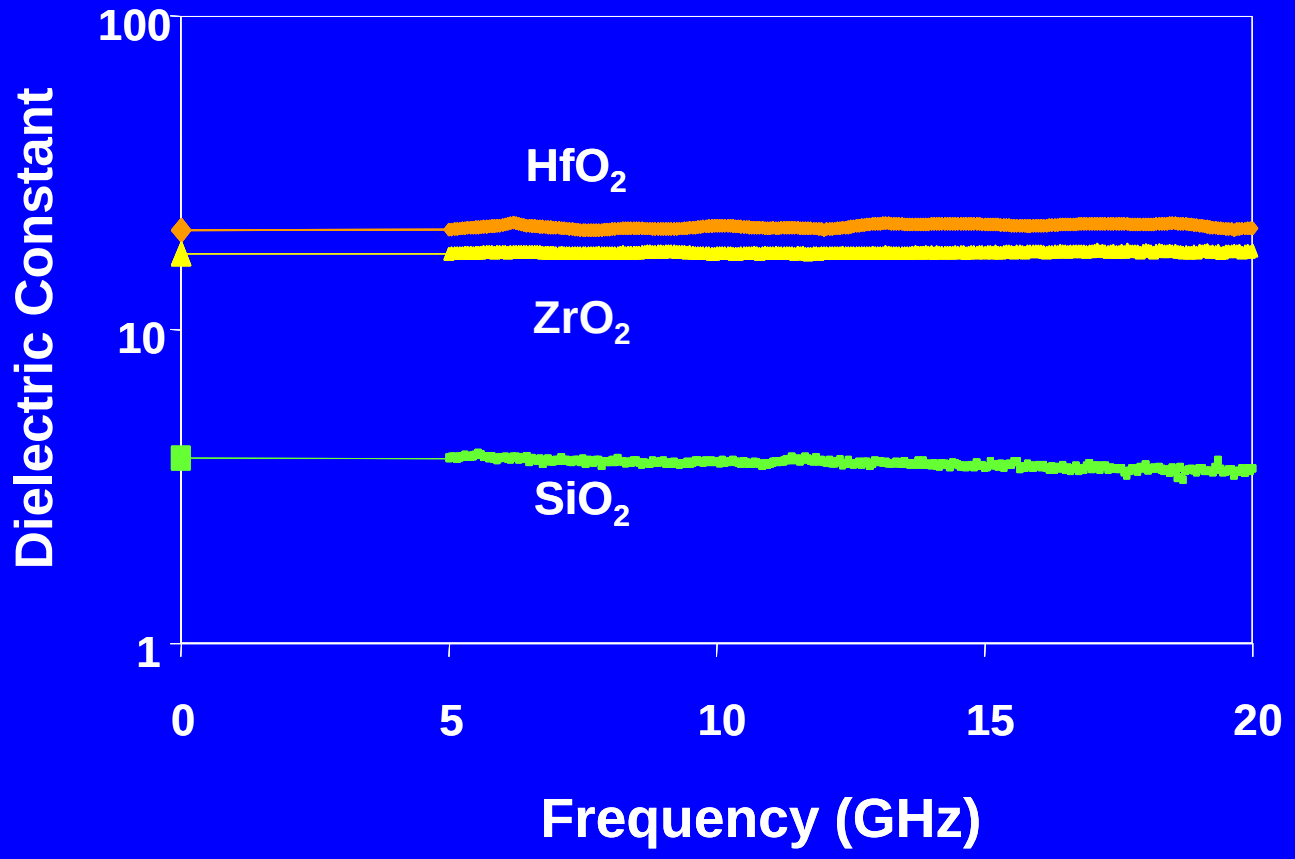
- **Minimize the total RC constant to maximize meaningful measurement Frequency**
  - **RC from Bussing – On wafer open short calibration**
  - **RC from Gate Width – Use small gate width and larger gate length**
  - **RC from Gate Length – Evaluate miller (overlap) capacitance**

High Frequency CV Curve



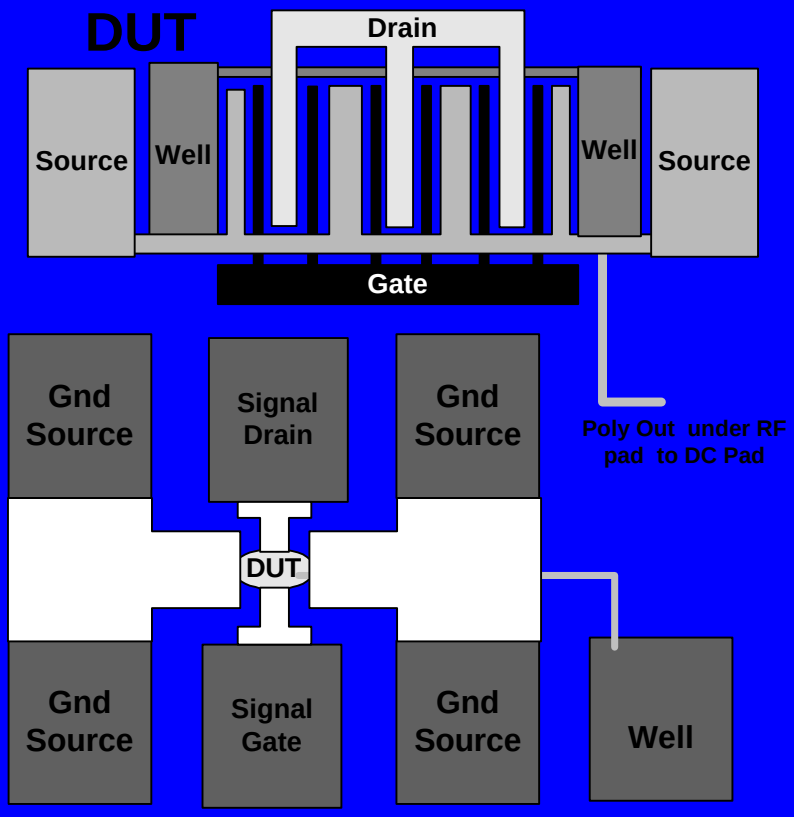
- The gate capacitance When $V_{gs} - V_{norm} = 0$, (miller capacitance or overlap capacitance) shows near zero dependence on frequency

Dielectric Constant Results

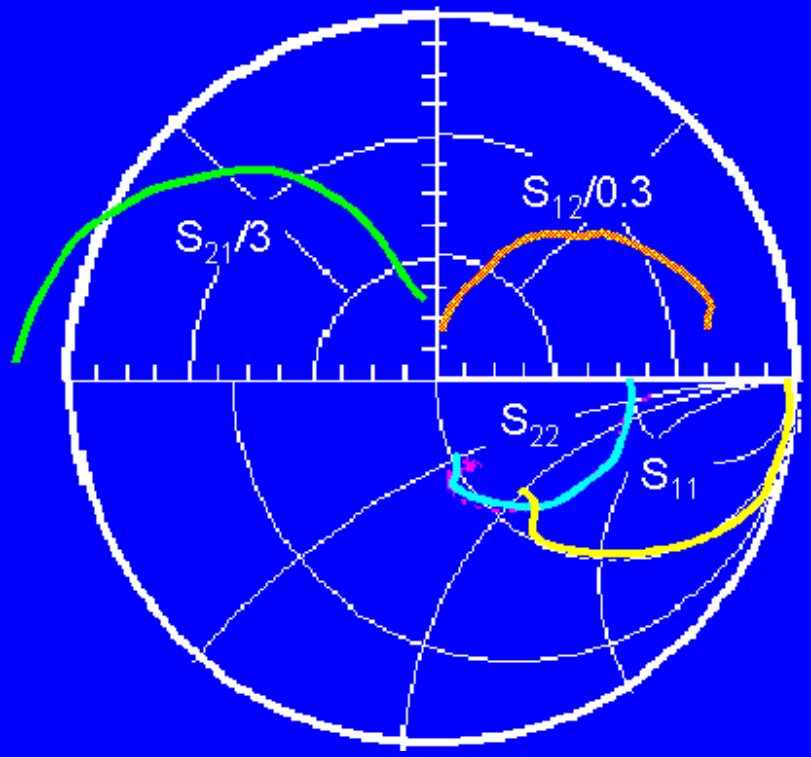


- Dielectric Constant Remains Invariant with respect to frequency for HfO_2, ZrO_2 and SiO_2

High Frequency Benchmark

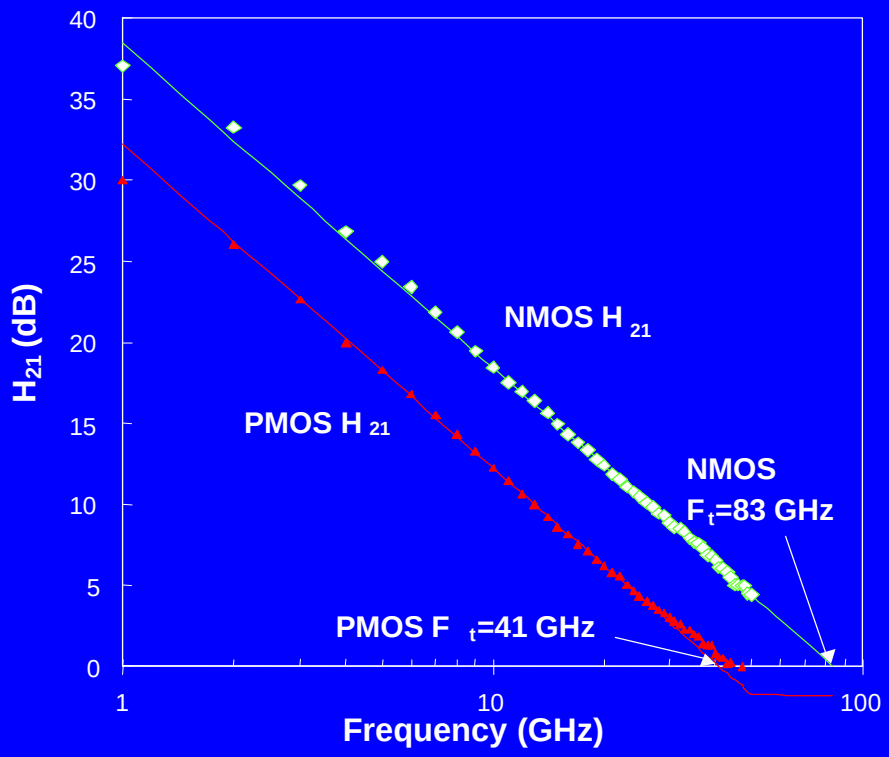


0.25 GHz-50.0GHz



- Use a reduced test transistor and a standard open-short de-embedding technique
- Gate length is 80nm and gate width is 6X7μm

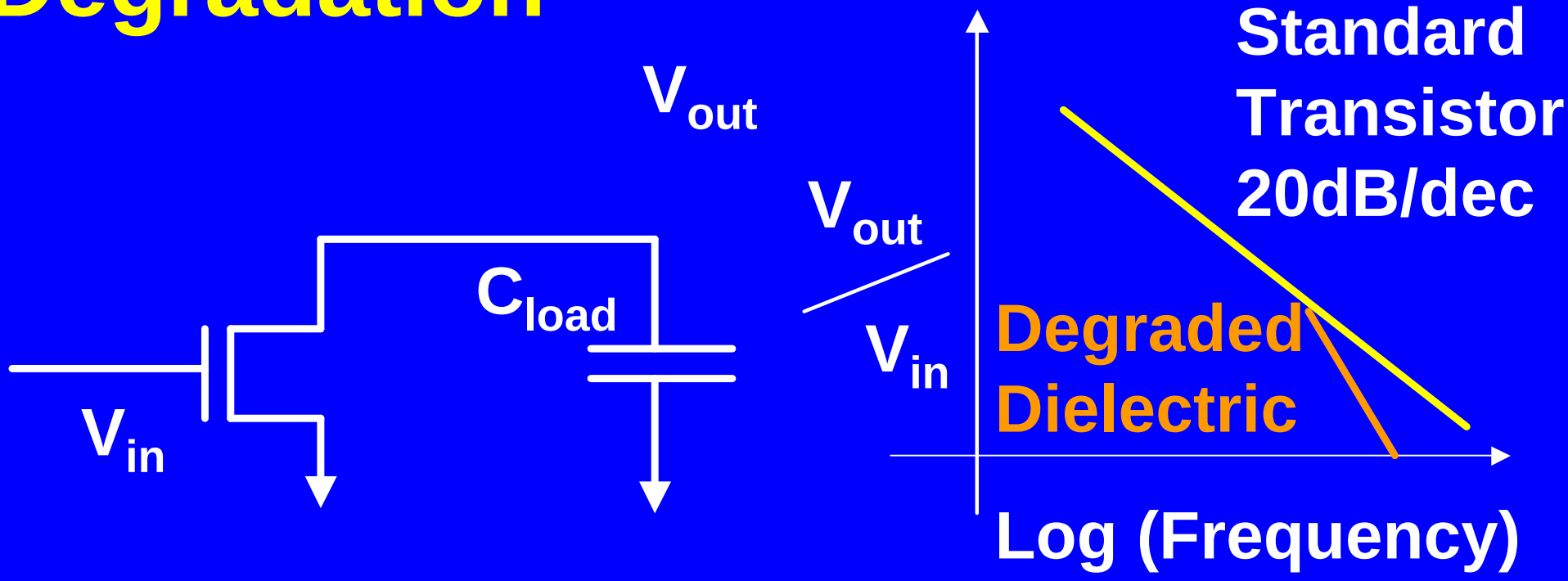
High Frequency Benchmark



	F_t	F_{max}
NMOS	83 GHz	39 GHz
PMOS	41 GHz	25 GHz

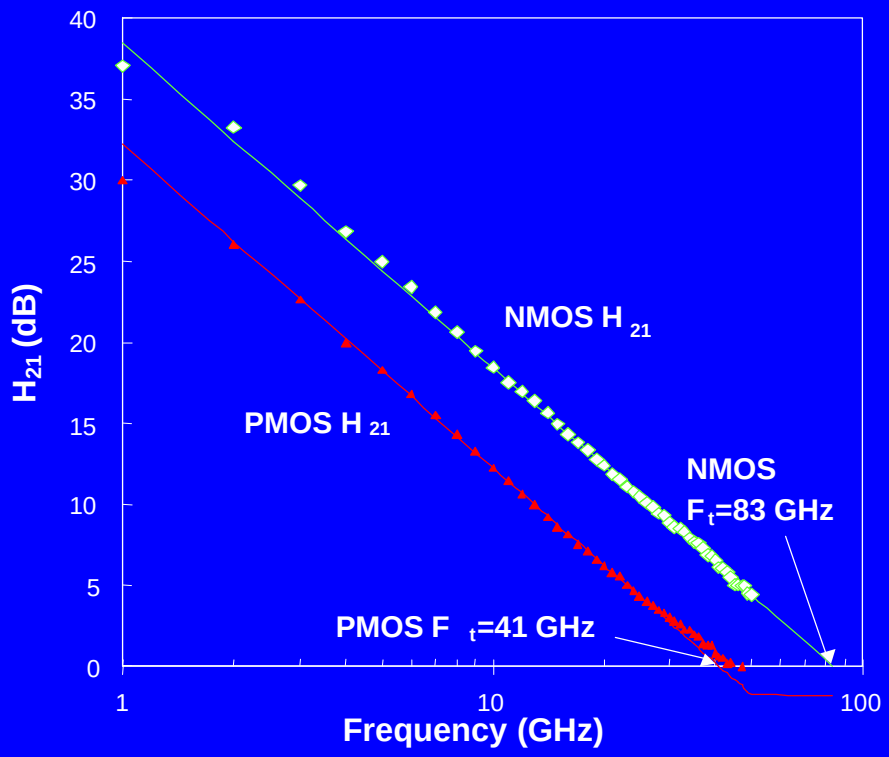
- H_{21} vs Frequency exhibits normal behavior up to 50GHz.

Motivation – Transistor Degradation



- The ability to drive a load at high speed will be lost if the dielectric constant degrades as a function of frequency

High Frequency Benchmark



	F_t	F_{max}
NMOS	83 GHz	39 GHz
PMOS	41 GHz	25 GHz

- H_{21} vs Frequency exhibits no abnormal degradation at higher frequencies

Conclusions

- For the first time, the high frequency benchmark for high-K/metal gate CMOS transistors is established
- The dielectric response of the high-K thin films is invariant with respect to frequency up to 20GHz
- The F_t for a Z/L = 7um/80nm high-K/metal gate device is 83 GHz for NMOS and 41 GHz for PMOS. The F_{max} is 39GHz for NMOS and 25GHz for PMOS
- The data suggests that high-K thin films are suitable for use as gate dielectrics in high frequency logic applications.

Acknowledgements

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- **Mark Bohr, Director of Process Architecture & Integration**
- **Youssef El-Mansy and Bill Holt, VPs and Directors of Logic Technology Development**

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